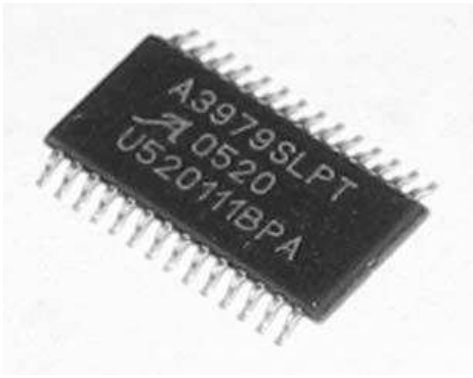
IMT-903 Microstep driver

(Allegro A3979SLP - T)

The IMT-903 provides maximum functional and power density with the least power loss with < 0.7 cm².



Advantages:

- Just 1 IC for power and logic up to 2.5 A and 35V provides maximum space and cost reduction with little external circuitry
- Microstep up to 1/16 provides quiet and even running behaviour and also reduces system resonance
- Automatic decay switchover (slow, mixed and fast) reduces power loss and motor noise considerably, and also increases step accuracy
- Extremely safe operation due to integrated overcurrent protection, undervoltage detection and crossover current protection

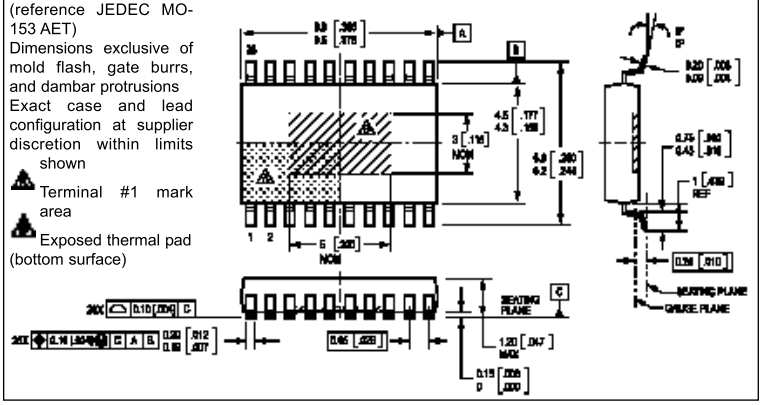
SMC11

Complete driver board with additional features: see SMC11

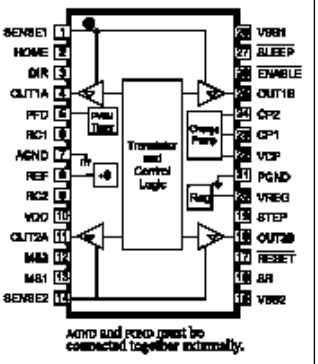
Complete information on the Internet:
www.nanotec.de

Dimensioned diagram (mm)

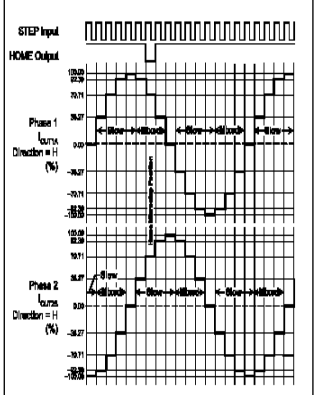
Dimensions in brackets = in
(reference JEDEC MO-153 AET)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
Terminal #1 mark area
Exposed thermal pad (bottom surface)



PIN assignments



Quarter step operation



Electrical characteristics

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 35 V, V_{DD} = 3.0 to 5.5 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	35	V
		During Sleep mode	0	–	35	V
Output Leakage Current[2]	I_{DSS}	V_{OUT} = V_{BB}	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<1.0	−20	µA
Output On Resistance	$R_{DS(ON)}$	Source driver, I_{OUT} = −2.5 A	–	0.26	0.336	Ω
		Source driver, I_{OUT} = 2.5 A	–	0.22	0.285	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = −2.5 A	–	–	1.4	V
		Sink diode, I_F = 2.5 A	–	–	1.4	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	8.0	mA
		Operating, outputs disabled	–	–	8.0	mA
		Sleep mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	12	mA
		Outputs off	–	–	10	mA
		Sleep mode	–	–	20	µA
Logic Input Voltage	$V_{IN(1)}$		0.7×V_{DD}	–	–	V
	$V_{IN(0)}$		–	–	0.3×V_{DD}	V
Logic Input Current[2]	$I_{IN(1)}$	V_{IN} = 0.7×V_{DD}	−20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.3×V_{DD}	−20	<1.0	20	µA
Reference Input Voltage Range	V_{REF}	Operating	0	–	V_{DD}	V
Reference Input Current	I_{REF}		–	0	±3	µA
HOME Output Voltage	$V_{HOME(1)}$	$I_{HOME(1)}$ = −200 µA	0.7×V_{DD}	–	–	V
	$V_{HOME(0)}$	$I_{HOME(0)}$ = 200 µA	–	–	0.3×V_{DD}	V
Mixed Decay Mode Trip Point	V_{PFDH}		–	0.6×V_{DD}	–	V
	V_{PFDL}		–	0.21×V_{DD}	–	V
Gain (G_m) Error[3]	E_G	V_{REF} = 2 V, Phase Current = 38.27%	–	–	±10	%
		V_{REF} = 2 V, Phase Current = 70.71%	–	–	±5.0	%
		V_{REF} = 2 V, Phase Current = 100.00%	–	–	±5.0	%
STEP Pulse Width	t_W		1	–	–	µs
Blank Time	t_{BLANK}	R_T = 56 kΩ, C_T = 680 pF	700	950	1200	ns
Fixed Off-Time	t_{OFF}	R_T = 56 kΩ, C_T = 680 pF	30	36	46	µs
Crossover Dead Time	t_{DT}	Synchronous rectification enabled	100	475	800	ns
Thermal Shutdown Temperature	T_{JSD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{JSDHYS}		–	15	–	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{DD}	2.45	2.7	2.95	V
UVLO Hysteresis	$V_{UVLOHYS}$		0.05	0.10	–	V

Block diagram

Input		Mode
MS1	MS2	
L	L	1/1 step
H	L	1/2 step
L	H	1/4 step
H	H	1/16 step